REMARKS

I. Status Of Claims

Claims 1-12 are pending in the present application and claims 1-12 stand rejected. Claims 1, 8, and 10-12 have been amended and claims 2-6 have been cancelled. Therefore, upon entry of this Amendment, claims 1 and 7-12 will be pending. No new matter has been introduced by the present Amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

II. Claim Rejections Under 35 U.S.C. § 102

Claims 1-7 and 12 stand rejected by the Examiner under 35 U.S.C. §102(e) as being anticipated by U.S Patent No. 6,091,617 to Moran (hereinafter, "Moran"). These rejections are respectfully traversed.

Claim 1 as now amended recites a PCI bus interface circuit for the voltage supply of a PCI plug-in card that can be connected to a PCI bus. Further, claim 1 recites that the PCI bus interface circuit comprises a first input for connection to a main voltage supply line of the PCI bus; a second input for connection to an auxiliary voltage supply line of the PCI bus; and an output for outputting a supply voltage to the PCI plug-in card. Claim 1 additionally recites that the PCI bus interface circuit comprises a first transistor, a second transistor, and a third transistor. The first transistor is for switching a main supply voltage that is present at the first input to the output, the first transistor having a first control terminal connected to the second input so that the first transistor switches

the main supply voltage that is present at the first input to the output if no auxiliary supply voltage V_{aux} is present at the second input. The second transistor is for switching an auxiliary supply voltage V_{aux} that is present at the second input to the output, the second transistor having a second control terminal connected to the first input so that the second transistor switches the auxiliary supply voltage that is present at the second input to the output if no main supply voltage V_{cc} is present at the first input. The third transistor, which, given the simultaneous presence of a main supply voltage V_{cc} at the first input and an auxiliary supply voltage V_{aux} at the second input, drives the second transistor for switching the auxiliary supply voltage V_{aux} through to the output, the third transistor being constructed complementarily with respect to the first and second transistors and having a third control terminal connected to the second input so that the third transistor, when an auxiliary supply voltage is applied to the second input, turns on and connects the second control terminal to a specific voltage potential with the result that the second transistor switches through the auxiliary supply voltage to the output. Summarily, Moran fails to teach or suggest all of the features of presently amended claim 1 for the reasons set forth hereinafter.

Moran is directed to a power supply system for a PCI adapter and discloses a PCI bus interface circuit for the voltage supply of PCI plug-in cards that can be connected to a PCI bus. The interface circuit comprises a first input for connection to a main voltage supply V_{CC}, a second input for connection to an auxiliary voltage supply line V_{aux}, and an output for outputting a supply voltage to the PCI plug-in card. The circuit of Moran further comprises a first (field effect) transistor Q3 for switching a main supply voltage

that is present at the first input to the output and a second (field effect) transistor Q2 for switching an auxiliary supply voltage that is present at the second input to the output.

Referring to Figure 2 of Moran, it is evident that the control terminal of transistor Q3 (i.e., the gate of the first (field effect) transistor Q3) is connected to the first input and not to the second input as recited in presently amended claim 1. In other words, the first transistor of the presently amended claim 1 (which is equivalent to the first (field effect) transistor Q3 of Moran) has a first control terminal connected to the second input, which is contrary to the first (field effect) transistor Q3 of Moran that has a control terminal connected to the first input.

It is additionally noted that the gates (control terminals) of the first and second (field effect) transistors Q3 and Q2, respectively, of the PCI bus interface circuit of Moran are connected to each other. As such, the first and second (field effect) transistors Q3 and Q2, respectively, of Moran are controlled in such a way that only one of the transistors is in its conducting state and the other is blocking. As a result, transistor Q1 of Moran, which corresponds to the third transistor in the presently amended claim 1, cannot be complementary with respect to both the first and second (field effect) transistors Q3 and Q2, respectively. This is contrary to presently amended claim 1 which recites that the third transistor is constructed complementarily with respect to the first and second transistors.

For these reasons, applicant respectfully submits that Moran does not disclose the PCI bus interface according to the present subject matter. Specifically, applicant

submits that Moran does not teach each and every element recited by the presently amended claim 1 and therefore does not anticipate the presently amended claim 1.

Claims 2-6 have been cancelled. Claim 12 depends from claim 1. Therefore, the comments presented above relating to claim 1 apply equally to claim 12.

Applicant respectfully submits that Moran does not teach or suggest each and every feature of the present subject matter, and therefore that pending claims 1 and 12 are not anticipated Moran. Applicant, therefore, respectfully requests that the rejection of claims 1 and 12 under 35 U.S.C. § 102(e) be withdrawn and the claims allowed at this time.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 8-11 stand rejected by the Examiner under 35 U.S.C. §103(a) as being unpatentable over Moran. These rejections are respectfully traversed.

As discussed above, Moran fails to teach or suggest the features of the presently amended claim 1, from which claims 8-11 depend. Specifically, the control terminal of transistor Q3 (i.e., the gate of the first (field effect) transistor Q3) of Moran (which is equivalent to the first transistor of the presently amended claim 1) is connected to the first input and not to the second input as recited in presently amended claim 1. Also, transistor Q1 of Moran, which corresponds to the third transistor in the presently amended claim 1, cannot be complementary with respect to both the first and second (field effect) transistors Q3 and Q2, respectively, since the first and second (field effect) transistors Q3 and Q2 are connected to each other. This is contrary to presently

amended claim 1 which recites that the third transistor is constructed complementarily with respect to the first and second transistors.

For these reasons, applicant respectfully submits that Moran does not teach or suggest each and every element recited by the presently amended claim 1. Since claims 8-11 depend from claim 1 and merely add additional limitations thereto, applicant also submits that Moran does not teach or suggest each and every element recited by claims 8-11 and therefore claims 8-11 are not obvious in view of Moran. Applicant, therefore, respectfully requests that the rejection of claims 8-11 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

CONCLUSION

In light of the above Amendments and Remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Office Action and/or Amendment.

DEPOSIT ACCOUNT

Although it is believed that no fee is due, the Commissioner is hereby authorized to charge any deficiencies of payment associated with the filing of this Response to Deposit Account No. **50-0426**.

Respectfully submitted,

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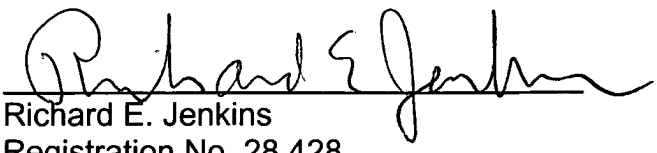
Date: January 31, 2006 By: 

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